

What is claimed is:

1. A semiconductor integrated device, comprising:

a memory cell holding bit information; a pair of bit lines
5 connected to the memory cell and used for inputting and outputting
said bit information in predetermined cycles; and

an output section that latches an output from said memory cell
via one bit line of the pair and the other bit line, and outputs said bit
information acquired from said one bit line as a result of reading from
10 said memory cell,

and pre-charging said pair of bit lines before access to said
memory cell,

wherein said memory cell has a cutoff circuit that cuts off said
other bit line to hold voltage thereof produced by pre-charging when
15 the bit information held in the memory cell is read out.

2. The semiconductor integrated device according to claim 1,

wherein said cutoff circuit is a switch, and the switch can
operate based on a switch control signal for switching off in
20 synchronism with the end of pre-charge in writing into said memory
cell, and switching on in synchronism with the start of pre-charge in a
next writing into said memory cell.

3. A semiconductor integrated device, comprising:

a memory cell holding bit information; a pair of bit lines
25 connected to the memory cell and used for inputting and outputting
said bit information in predetermined cycles; and

an output section that outputs said bit information held in said memory cell via said bit line pair to the outside,

and pre-charging said bit line pair before access to said memory cell,

5 said semiconductor integrated device further comprising:

 a cutoff section that keeps connection between the bit line pair pre-charged to write new bit information into said memory cell and said output section cut off until a next writing.

10 4. A semiconductor integrated device, comprising:

 memory cells holding bit information; and

 a pair of bit lines connected to the memory cells and used for inputting and outputting said bit information in predetermined cycles, and pre-charging said bit line pair for access to said memory

15 cells, said semiconductor integrated device further comprising:

 an equalizer that cuts the bit line pair pre-charged in the former readout in two consecutive cycles of readout for bit information held in the memory cells off from pre-charge potential supply ports and equalizes, in the next readout, respective potentials held in said
20 bit lines of the bit line pair by the cutoff.

5. A semiconductor integrated device, comprising:

 memory cells holding bit information; and

25 a pair of bit lines connected to the memory cells via which said bit information is input and output in predetermined cycles,

 and pre-charging said bit line pair for access to said memory cells,

said semiconductor integrated device further comprising:

an equalizer that cuts the bit line pair pre-charged in the former access in two consecutive cycles of access for the memory cells off from pre-charge potential supply ports and equalizes, in the next
5 access, respective potentials held in said bit lines of the bit line pair by the cutoff.